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<tr>
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<td></td>
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<td>AoE</td>
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<td>CoE</td>
<td>CANopen over EtherCAT</td>
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<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
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<tr>
<td>DC</td>
<td>Distributed Clocks</td>
<td></td>
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<tr>
<td>DPRAM</td>
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<td></td>
</tr>
<tr>
<td>ENI</td>
<td>EtherCAT Network Information (network configuration in XML format)</td>
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<tr>
<td>EoE</td>
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<tr>
<td>ESM</td>
<td>EtherCAT State Machine</td>
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<td>Ethernet for Control Automation Technology</td>
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<tr>
<td>FMMU</td>
<td>Fieldbus Memory Management Unit</td>
<td></td>
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<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
<td></td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose I/O</td>
<td></td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group</td>
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<tr>
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<tr>
<td>LVDS</td>
<td>Low Voltage Differential Signaling</td>
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<tr>
<td>M</td>
<td>Meaning</td>
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</tr>
<tr>
<td>MII</td>
<td>Media Independent Interface</td>
<td></td>
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<tr>
<td>NIC</td>
<td>Network Interface Controller</td>
<td></td>
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<td>NVRAM</td>
<td>Non Volatile Random Access Memory</td>
<td></td>
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<td>OEM</td>
<td>Original Equipment Manufacturer</td>
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<td>PDI</td>
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<td>PIC</td>
<td>Programmable Integrated Circuit</td>
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<td>PLC</td>
<td>Programmable Logic Controller</td>
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<tr>
<td>RMII</td>
<td>Reduced Media Independent Interface</td>
<td></td>
</tr>
<tr>
<td>SII</td>
<td>Slave Information Interface</td>
<td></td>
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<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
<td></td>
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<tr>
<td>TCP/IP</td>
<td>Transmission Control Protocol/Internet Protocol</td>
<td></td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
<td></td>
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<td>XML</td>
<td>Extended Markup Language</td>
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1 Preface

This document describes from a very practical point of view which topics have to be kept in mind for a successful EtherCAT® slave implementation. It answers the following questions:

- What is the general structure of an EtherCAT slave device?
- What kinds of EtherCAT Slave Device Controllers are available? What are the differences?
- What Evaluation Boards are available and what are their features?
- Is EtherCAT training available?
- Which documents are needed or helpful and how can they be accessed?
- Is there a technical support?
- Why attend a Plug Fest?
- Is a Conformance Test available? How does it work?
- What steps have to be done for an EtherCAT slave implementation?

There are definitely other possibilities how such an implementation can be done, however, the way it is described in the following document has proofed many times to lead very fast to an EtherCAT slave device implementation of high quality.

Prior to publishing this version, all ETG members that offer EtherCAT development products, EtherCAT implementation services and EtherCAT workshops known to the ETG were asked to contribute their offers to this guideline. If you are aware of missing information, please provide this to info@ethercat.org to enhance this guide. Feedback or other suggestions are also welcome.

This version of the document is based on information available by May 2009.
2 EtherCAT Slave Structure

Figure 1 shows the EtherCAT Slave Structure and how it is connected to an EtherCAT master.

![EtherCAT Slave Structure](image)

**EtherCAT Master / Configuration Tool**

Not part of the Slave. The Configuration Tool is used to generate a network description, the so called EtherCAT Network Information file (ENI, XML file based on a pre-defined file schema) based on the information provided by the EtherCAT Slave Information file (ESI, device description in XML format) and/or the EEPROM and/or object dictionary.

The ENI file describes the network topology, the initialization commands for each device and the commands which have to be sent cyclically. The ENI file is provided to the master, which sends the commands according to this file.

The only hardware requirement for an EtherCAT master is a standard NIC.

**EtherCAT Slave structure parts:**

**EtherCAT Slave Information File**

Every EtherCAT device shall be delivered with an EtherCAT Slave Information (ESI) file in XML format. It describes the identity and all features of the device.

**Slave Hardware**

The slave hardware consists of the following parts:

- Standard Ethernet Physical Layer Components
- EtherCAT Slave Controller (ESC) and EEPROM (ESC configuration data and application specific data)
- For intelligent slaves with an application controller: Host controller

**Standard Ethernet Physical Layer Components**

The physical layer is based on the standards defined by standard Ethernet according to IEEE802.3. This means Standard Ethernet components:

- Plugs (RJ45 or M12)
- Magnetics
- PHYs
In order to maximize the EtherCAT performance, it is required to select the PHYs according to the criteria listed in the ESC data sheets.

For EtherCAT devices connected to an internal backbone connection, LVDS can be used as Physical Layer. This Physical Layer is also called “E-bus”. Then Magnetics and PHYs are no longer required, the connectors are vendor specific.

**EtherCAT Slave Controller (ESC)**

The ESC can either be implemented as FPGA or ASIC. This hardware handles the EtherCAT protocol in real-time. Thus, the performance of the EtherCAT communication does not depend on the implementation of the application software in the host controller. Neither does the communication speed have impact on the performance of the application controller.

To connect the ESC to an application controller or just digital I/Os the following Process Data Interfaces (PDI) are available depending on the ESC type:

- 32 Bit digital I/O
- Serial Peripheral Interface (SPI)
  - Used for small process data
- 8/16-bit synchronous/ asynchronous MicroController Interface (MCI)
  - Usually used for larger process data

Process data and parameter data are exchanged via a DPRAM while the ESC behaves like a memory. Appropriate mechanisms are provided by the ESC hardware (defined by the EtherCAT protocol) to ensure data consistency.

**EEPROM / SII**

During start-up the ESC needs to load configuration data (e.g. PDI type) from an external NVRAM. Most ESC support an I²C interface to connect an EEPROM. This interface is called Slave Information Interface (SII).

**Application Layer/ Host controller**

In a complex slave the application layer services are implemented on an application controller here named as host controller.

The host controller has to support the following tasks:

- EtherCAT State Machine (ESM) handling
- Process data – Exchange with the application
- Mailbox protocols (CoE, EoE, etc.)
- Object Dictionary Handling
- Handling of Application Parameter (Communication Parameter are handled by ESC)
- Optional TCP/IP Stack Handling – if device supports EoE
- µC-Performance is determined by device application, not by EtherCAT communication.
  - In many cases an 8-bit µC / PIC is sufficient
3 EtherCAT Slave Controller (ESC) Variants

An EtherCAT Slave Controller (ESC) can either be implemented as FPGA or ASIC.

Possible criteria for the choice of one device:

- Number and Type of Ports (MII, E-bus)
- PDI Type (functionality, speed)
  - Simple devices
    - Digital I/O Interface (up to 32 Bit I/O)
  - Complex devices
    - Serial Peripheral Interface (SPI)
    - 8/16-bit synchronous/ asynchronous MicroController Interface (MCI)
- RAM size (depending on the size of process data and mailbox data)
- Number of SyncManagers and FMMUs
- A usual device uses:
  - One SyncManager per acyclic data output (mailbox out), acyclic data input (mailbox in), cyclic data output (process data out), cyclic data input (process data in)
  - One FMMU per cyclic output data block, cyclic input data block, optionally one additional for mapping the "mailbox response available" flag into process data (no polling of mailbox necessary)
- Distributed Clocks (DC) for synchronization
- Needed quantity, flexibility in relation to price

Table 1 lists all ESC variants available on the market by March 2009.
## Table 1: EtherCAT Slave Controller Overview

<table>
<thead>
<tr>
<th>Name</th>
<th>ET1100</th>
<th>ET1200</th>
<th>ET1810/ET1811/ET1812</th>
<th>ET1815/ET1816/ET1817</th>
<th>netX 5</th>
<th>netX 100</th>
<th>netX 500</th>
<th>netX50</th>
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<tr>
<td>Type</td>
<td>ASIC</td>
<td>ASIC</td>
<td>FPGA + IP Core</td>
<td>FPGA + IP Core</td>
<td>ASIC</td>
<td>ASIC</td>
<td>ASIC</td>
<td>ASIC</td>
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<tr>
<td>Hardware Supplier</td>
<td>Beckhoff</td>
<td>Beckhoff</td>
<td>Altera (Cyclone I+II+III, Stratix I+II+III+IV +GX+II GX, Arria GX)</td>
<td>Xilinx (Spartan 3+3E+3A+3AN+3ADSP, Virtex I+II Pro+II Pro X+4+5)</td>
<td>Hilscher</td>
<td>Hilscher</td>
<td>Hilscher</td>
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<td>QFN48 0,5mm Pitch</td>
<td>FPGA dependent</td>
<td>FPGA dependent</td>
<td>BGA201 0,8mm pitch</td>
<td>BGA345 1mm Pitch</td>
<td>BGA345 1mm Pitch</td>
<td>PBGA 1mm Pitch</td>
</tr>
<tr>
<td>Size</td>
<td>10 x 10 mm</td>
<td>7 x 7 mm</td>
<td>FPGA dependent</td>
<td>FPGA dependent</td>
<td>13 x 13 mm</td>
<td>22 x 22 mm</td>
<td>22 x 22 mm</td>
<td>19 x 19 mm</td>
</tr>
<tr>
<td>µC Interface</td>
<td>serial/parallel (8/16-bit, async)*</td>
<td>serial*</td>
<td>serial/parallel (8/16-bit, async) AVALON®*</td>
<td>serial/parallel (8/16-bit, async) OPB®*</td>
<td>serial (SPI), parallel (8/16/32, async)</td>
<td>µC-Bus (internal, 32-bit)</td>
<td>µC-Bus (internal, 32-bit)</td>
<td>µC-Bus (internal, 32-bit)</td>
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<td>Digital I/O</td>
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<td>8-32*</td>
<td>8-32*</td>
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<td>16 (GPIO)</td>
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<td>32 (GPIO)</td>
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<td>DPRAM</td>
<td>8 kByte</td>
<td>1 kByte</td>
<td>1...60 kByte*</td>
<td>1...60 kByte*</td>
<td>6 kByte</td>
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<td>256/400 Byte (Mailbox/Process Data)</td>
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<td>0...8*</td>
<td>8</td>
<td>4</td>
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<td>8</td>
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<td>FMMU Entities</td>
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<td>0...8*</td>
<td>0...8*</td>
<td>8</td>
<td>3</td>
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<td>Distributed Clock Support</td>
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<td>yes</td>
<td>yes*</td>
<td>yes*</td>
<td>Yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
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<tr>
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<td>2-4 (MII/E-bus)*</td>
<td>2-3 (E-bus/ max. 1x MII)*</td>
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<td>2 (MII)</td>
<td>2 (MII)</td>
<td>2 (100BASE-TX)</td>
<td>2 (100BASE-TX)</td>
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<td>Specials</td>
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<td>Several IP Core License models available</td>
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</tbody>
</table>

*configurable

Further Information: [http://www.beckhoff.de/english/ethercat/ec_entwicklungsprodukte_overview.htm?id=3557177466](http://www.beckhoff.de/english/ethercat/ec_entwicklungsprodukte_overview.htm?id=3557177466)

Data Sheets: [http://www.beckhoff.de/english/download/ethercat_development_products.htm](http://www.beckhoff.de/english/download/ethercat_development_products.htm)
Comments on Table 1:

SyncManager
A SyncManager entity manages the DPRAM access from EtherCAT and application controller side so that data consistency is ensured on both sides.

FMMU
The Fieldbus Memory Management Units (FMMU) are used to map process data from the logical process data image on the EtherCAT master to the physical memory of the local device. Thus, process data mapping on the master is not necessary anymore and a significant lot of CPU power is saved on an EtherCAT master compared to legacy fieldbusses.

User Memory
An ESC provides 4 kByte of register memory (address 0x0000 to 0x0FFF). Mailbox data and process data are exchanged via a DPRAM memory, the so called User Memory. EtherCAT Addressing services allow to address user memory up to 60 kBytes. ESCs have between 1 kByte and 8 kByte RAM, IP Cores can be configured to provide the full 60 kByte user memory.

Ports
The physical layer of EtherCAT is based on standard Ethernet. Thus, standard MII is supported for stand alone devices connected to one another via CAT 5 cables. For more space and price sensitive devices such as modular devices another physical layer for EtherCAT is used, the so called EBUS. The EtherCAT protocol remains unchanged, only the physical form is changed.

A stand alone device needs to support at least two MII ports. This is one of the main differences between the several ESC types.

IP-Core Licenses
The EtherCAT IP core enables the EtherCAT communication function and application-specific functions to be implemented on an FPGA (Field Programmable Gate Array). The EtherCAT functionality is configurable with regards to the EtherCAT features such as number of FMMUs and SyncManagers, DC support, PDI.

A plug-in for Altera or Xilinx development environment is available to configure the core.

Different License models are support for both supported FPGA devices, Altera and Xilinx:

- EtherCAT IP Core, unlimited, “node-locked license”
  This license allows to use the configurable EtherCAT IP Core for as many EtherCAT devices as desired, but the installation is restricted to one workstation.

- EtherCAT IP Core, unlimited, “floating license”
  This server license allows using the configurable EtherCAT IP Core for as many EtherCAT devices as desired and can be used by several workstations, but restricts the access to one workstation at the same time. There are upgrade options to use the license on different workstations at the same time.

- EtherCAT IP Core, quantity-based, “node-locked license”
  This quantity-based license offers manufacturers of small lots and development service providers the possibility to development EtherCAT IP Core devices with low initial investment.

  For the development of an EtherCAT device, a one-time kick-off charge is required, plus the royalty for 1,000 devices. Development service providers only require the one-time kick-off charge; a system integrator OEM license is required for each customer implementation. The end customer then needs the royalty license.
4 EtherCAT Implementation

4.1 Slave Evaluation Boards

This list might not always be complete as new products are brought to the market without becoming known to the ETG. More products might be listed by the product guide at: www.ethercat.org → Products → Development Systems, Tools and Services.

Evaluation Boards are listed in alphabetical order.

4.1.1 Beckhoff EtherCAT Evaluation Kit EL98xx

With the Evaluation Kit (base board EL9800 with EtherCAT piggyback controller board) a one-day hands-on workshop and a preceding one day training class explaining the EtherCAT protocol are offered. See also clause 4.1.4.

Scope of delivery is described in Table 2.

Table 2: EL9800 - Scope of Delivery

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
</tr>
</thead>
</table>
| EL98xx       | Base board with:  
  - Socket for FB11xx EtherCAT Piggyback Board with EtherCAT Slave Controller  
  - Several PDI (32 Bit Digital I/O, 8/16-bit µC, SPI) to connect the desired hardware  
  - On-board PIC connected via SPI to ESC with pre-installed Slave Sample Code  
  - Debugger Interface for MPLAB®  
  - Power supply (24V)  
  - Cables, Documentation |
| SSC          | EtherCAT Slave Sample Code  
  C-Code as framework of an EtherCAT application including:  
  - Handling of synchronous and asynchronous data exchange via DPRAM  
  - Support of mailbox protocols (CoE incl. Object Dictionary, EoE, FoE, AoE)  
  - Support of synchronized application using Distributed Clocks |
| Piggyback Board | Slave Controller Board, equipped with different ESC (ASIC or FPGA variants) and configurable to several PDI.  
  For detailed information of the different ordering options please see clause 4.2.1 |
| ESI          | EtherCAT Slave Information (Device Description) in XML format necessary for every slave |
| TwinCAT      | Full EtherCAT Master with integrated EtherCAT hardware configuration tool and PLC development environment (license included but limited to the use in conjunction with the evaluation board) |

Figure 2 shows the evaluation board with mounted EtherCAT Slave Controller Board (FB11xx).
4.1.2 EBV DBC3C40 (Mercury Code)

The DBC3C40 is a Cyclone III Development Board with several I/O transceivers for industrial communication purposes. Former version of this board is DBC2C20 with Altera Cyclone II.

The following features are integrated:

- EP3C40F484C7N
- 2 x 10/100 Ethernet PHY
- LVDS TFT interface
- 16 Mbyte SDRAM
- 1Mbyte SRAM
- 8 Mbyte flash
- Security Eprom
- 1 x UART transceiver
- 2 x CAN transceiver
- 4 x RS485 transceiver
- USB 2.0 OTG
- Temperatur Sensor
- 32 pin I/O connector
- 16 bit 24V I/O interface
- 8 x User LEDs
- 2 digit seven segment display
- 4 user buttons
- navigation key
- on board 12V, 5V, 3.3V, 2.5V, 1.2V power supply
Further information:

4.1.3 Hilscher netX100 Network Evaluation Board

Together with a protocol stack, the Network Evaluation Board works as Master or Slave in the network. It allows data exchange via switches, LEDs and performance measurements. Furthermore, it serves as reference for the certification and circuit example for other fieldbus and the various Real-Time Ethernet systems.

- netX 100 controller with Master License
- 4 MByte 16-Bit Flash
- 8 MByte 32-Bit SDRAM
- Two Ethernet Ports with Switch and Hub Functionality
- Fieldbus Interface for AS-Interface (Master only), CANopen, CC-Link, DeviceNet, InterBus (Master only), PROFIBUS
- USB 1.1 Device
- RS232C-Interface
- JTAG-Interface
- 16 Switches as Digital Inputs
- 16 LEDs as Digital Outputs
- Two Digit Address Switch
- Reset and Boot Buttons

Further information:
http://uk.hilscher.com/products_details_hardware.html?p_id=P_437b5c89e0676&bs=15
4.1.4  Hilscher NXHX 500-RE Evaluation Board

- Interfaces: I/O, parallel host interface, UART, USB
- Sample Code: EtherCAT Slave Hardware Abstraction Layer (HAL) available on demand
- Specials: DIP-switches and LEDs for I/O, SD card slot, fieldbus interface (optional), Multi-protocol support

The netX network controller with its 32 Bit / 200 MHz ARM CPU provides a high degree of computing performance and comprehensive peripheral functions for single chip solutions in price-sensitive applications. Here the network protocols and the application program together use the resources of the netX and are carried out together in a Real-Time operating system.

The simplest and most economic way of evaluating the whole system is with the netX software development board. Besides a universal hardware, it also possesses an integrated debug interface and is supplied with the HiTOP development environment from Hitex.

Your application can be loaded onto the board and run with our protocol stacks and, for instance, combined with the licence-free rcX Real-Time Kernel.

For this purpose HiTOP, having integrated the GNU compiler, offers a comfortable development and debugging environment. Code can be developed without limitation. However, using the HiTOP supplied testing is only possible on the software development board. With the exception of the debug interface you will receive the complete circuit diagram providing a basis for your hardware development. On this hardware you will later connect, via the JTAG Interface, the Tantino from Hitex and test or develop with the same user interface and functionality as on the development board.

Figure 5: Hilscher NXHX 500-RE

Further information:
http://uk.hilscher.com/products_details_hardware.html?p_id=P_461ff2053bad1
4.2 Slave Communication Modules

This list might not always be complete as new products are brought to the market without becoming known to the ETG. More products might be listed in the product guide of the EtherCAT website: www.ethercat.org → Products → Development Systems, Tools and Services.

Slave Communication Modules are listed in alphabetical order.

4.2.1 Beckhoff FB11xx

The FB11xx EtherCAT piggyback controller boards offer complete EtherCAT connection based on the ET1100 EtherCAT ASIC or an Altera or Xilinx FPGA in conjunction with the ET18xx EtherCAT IP core. All FB11xx have the same form factor and can be used with the EL98xx EtherCAT Evaluation Kit. They can be integrated as EtherCAT interfaces in devices.

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB1111-0140</td>
<td>EtherCAT piggyback controller board with ET1100 (ASIC) and µC interface; can be integrated as EtherCAT interface in devices.</td>
</tr>
<tr>
<td>FB1111-0141</td>
<td>EtherCAT piggyback controller board with ET1100 (ASIC) and SPI interface; can be integrated as EtherCAT interface in devices.</td>
</tr>
<tr>
<td>FB1111-0142</td>
<td>EtherCAT piggyback controller board with ET1100 (ASIC) and digital I/O interface; can be integrated as EtherCAT interface in devices; included in the EL982x evaluation kit and together with the delivered adapter card EL9803 all interfaces (µC, SPI, digital I/O) can be used. This is the most flexible solution for starting an EtherCAT implementation.</td>
</tr>
<tr>
<td>FB1122</td>
<td>EtherCAT piggyback controller board with Altera Cyclone III (FPGA); included in the EL9830 evaluation kit; IP Core licence necessary</td>
</tr>
<tr>
<td>FB1130</td>
<td>EtherCAT piggyback controller board with Xilinx Spartan-3E XC3S1200E (FPGA); included in the EL9840 evaluation kit; IP Core license necessary</td>
</tr>
</tbody>
</table>

4.2.2 Hilscher comX

- Interfaces: Host processor over dual-ported memory (parallel)
- Ports: 2 (100BASE-TX)

All stacks are implemented as slave protocols and are executed on the comX-Module. Data exchange with the host application is carried out via Dual-Port-Memory interface. The process data images are available directly via memory read and write functions. The comX Module features two RJ45 connectors for Ethernet. netX based comX-Modules gets it's identity by loading an appropriate firmware file.

- All Real-Time-Ethernet System use netX Network Controller
- Available as Master and Slave
- Two Ethernet Ports with Switch and Hub for Line Topology
- System/Status/Link/Activity LEDs
- 8 or 16-Bit Host Application Interface
- USB & UART Diagnostic Interface
- Direct Process Data Access
- Same Dimensions and Pin Compatible like our well-known COM-C Module
- SYCON.net as configurator based on FDT/DTM
- Short 'Time-To-Market'

![Figure 7: Hilscher comX module](http://uk.hilscher.com/products_group_embeddedsolutions.html)
4.3 Workshop and Training

The following trainings are offered additionally to the Beckhoff Evaluation Board:

Table 4: EL9800 - Workshop and Training

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EtherCAT technology basics for developers TR8110</td>
<td>One day training class handles:</td>
</tr>
<tr>
<td></td>
<td>• EtherCAT Basics</td>
</tr>
<tr>
<td></td>
<td>• Slave Structure</td>
</tr>
<tr>
<td></td>
<td>• Physical Layer</td>
</tr>
<tr>
<td></td>
<td>• Protocol</td>
</tr>
<tr>
<td></td>
<td>• Application Layer features including device profiles</td>
</tr>
<tr>
<td></td>
<td>• Distributed Clocks</td>
</tr>
<tr>
<td></td>
<td>• Device description in XML format (ESI)</td>
</tr>
<tr>
<td></td>
<td>• Master and slave implementation questions</td>
</tr>
<tr>
<td></td>
<td>• Overview standards and references</td>
</tr>
<tr>
<td>EtherCAT evaluation workshop for slave developers TR8100</td>
<td>One day hands-on workshop includes:</td>
</tr>
<tr>
<td></td>
<td>• EtherCAT hardware</td>
</tr>
<tr>
<td></td>
<td>• Installation of TwinCAT, incl. drivers</td>
</tr>
<tr>
<td></td>
<td>• Handling of PDI</td>
</tr>
<tr>
<td></td>
<td>• Slave Sample Source Code</td>
</tr>
<tr>
<td></td>
<td>• ESC device overview (ET1100, ET1200, IP Core)</td>
</tr>
<tr>
<td></td>
<td>• Device description in XML format (ESI)</td>
</tr>
</tbody>
</table>

Both offered workshop and training class have proved to put the developer in a good starting position with a basic understanding of the EtherCAT protocol, EtherCAT tools, development hardware and software including the Slave Sample Code as a basis to build the vendor specific application on top.

Further information:
http://www.beckhoff.com/english/support/tr8110_tr8100_tr8200.htm

For other EtherCAT workshops and trainings please see:
www.ethercat.org → Events
4.4 Documentation

Table 5 lists the fundamental documents about the EtherCAT technology. This list does not cover all EtherCAT documentation. For a complete list of all available EtherCAT documentation please see: www.ethercat.org → Downloads.

<table>
<thead>
<tr>
<th>Document</th>
<th>Description and Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proceedings of ETG Events</td>
<td>Minutes of the Technical Committee Meetings and Member Assemblies: → <a href="http://www.ethercat.org">www.ethercat.org</a> → Member Area → Downloads: Proceedings of ETG Events</td>
</tr>
<tr>
<td>EtherCAT Indicator Specification</td>
<td>Description of the required LEDs of an EtherCAT device: → <a href="http://www.ethercat.org">www.ethercat.org</a> → Member Area → Downloads: EtherCAT Specification</td>
</tr>
<tr>
<td>Drive Profiles and Mapping to EtherCAT CiA402 Implementation Guideline</td>
<td>Additional information on the Drive Profile and Mapping to EtherCAT specification: → <a href="http://www.ethercat.org">www.ethercat.org</a> → Member Area → Downloads: EtherCAT Specification</td>
</tr>
<tr>
<td>EtherCAT Slave Information (ESI) Schema and Specification</td>
<td>The EtherCAT Device Description specifies the structure in XML format: → <a href="http://www.ethercat.org">www.ethercat.org</a> → Member Area → Downloads: EtherCAT Specification The Schema describes the structure in XML format: → <a href="http://www.ethercat.org">www.ethercat.org</a> → Member Area → Downloads: EtherCAT Slave</td>
</tr>
<tr>
<td>EtherCAT Network Information (ENI) Schema and Specification</td>
<td>The EtherCAT Network Information (ENI) file specifies the structure of an EtherCAT network in XML format (this file can be created by the master or a separate configuration tool): → <a href="http://www.ethercat.org">www.ethercat.org</a> → Member Area → Downloads: EtherCAT Specification The Schema describes the structure in XML format: → <a href="http://www.ethercat.org">www.ethercat.org</a> → Member Area → Downloads: EtherCAT Master</td>
</tr>
<tr>
<td>Data Sheets for Beckhoff ESCs</td>
<td>Detailed description of the EtherCAT Slave Controllers including a description of basic EtherCAT mechanisms and how they work within the ESC: → <a href="http://www.beckhoff.de/english/download/ethercat_development_products.htm">www.beckhoff.de/english/download/ethercat_development_products.htm</a></td>
</tr>
<tr>
<td>Data Sheets for Beckhoff EtherCAT IP-Cores (Altera/Xilinx)</td>
<td>Detailed description of the ESC IP Core for Altera and Xilinx FPGAs including a description of basic EtherCAT mechanism and how they work within the ESC: → <a href="http://www.beckhoff.de/english/download/ethercat_development_products.htm">www.beckhoff.de/english/download/ethercat_development_products.htm</a></td>
</tr>
<tr>
<td>Data Sheets for Hilscher ESCs</td>
<td>Detailed description and features of the netX product family: → <a href="http://www.hilscher.com/netx.html">www.hilscher.com/netx.html</a> → Further Information → netX Datasheet</td>
</tr>
</tbody>
</table>
4.5 Plug Fest

Depending on the demand of ETG companies Plug Fests are held at least two times a year. Every ETG member developing devices or tools with at least a functional prototype are allowed to attend. In practical tests interoperability and the latest features of the devices are tested and the EtherCAT Slave Conformance Test tool is used. Qualified feedback of EtherCAT specialists is provided.

Dates are published within the Events section at [www.ethercat.org](http://www.ethercat.org). An additional invitation is automatically sent to the ETG representative of the ETG member company by email.

4.6 Technical Committee

At least twice a year the Technical Committee (TC) of the ETG meets, typically in March and September. Hence the meeting serves as central technical board, establishes work groups, task forces and receives their report. Other duties of the TC is to inform about enhancements of the EtherCAT technology, progress on standardization and serving to discuss current technical issues with all attending ETG members.

Dates are published within the Events section at [www.ethercat.org](http://www.ethercat.org). An additional invitation is automatically sent to the ETG representative and former attendees of the ETG member company by email.

4.7 Conformance

Conformance and interoperability are very important factors for the success of a communication technology. Conformance of the technology implementation with the specifications is the pre-requisite of interoperability, which means that devices of different manufacturers co-operate within the same networked application.

The conformance testing rules and policies according to the Vendor ID agreement are covered by the Conformance Test Policy, which can be downloaded at [www.ethercat.org/download/conformance](http://www.ethercat.org/download/conformance).

**Developing a conform device with the Conformance Test Tool**

The Conformance Test Tool allows checking protocol compliance in-house. Vendors are encouraged to use the tool throughout their development process to eliminate protocol deviations in an early stage. See Table 6 how to access the tool.

**Obtain an EtherCAT Conformance Tested Certificate**

To apply for the EtherCAT Conformance Test at any EtherCAT Test Center (ETC) send an Email to Conformance@EtherCAT.org to ask for further information and the Request Form. On return of the Request Form to the ETG the requested ETC will contact you for further steps.

The Conformance Guide ([www.ethercat.org/download/conformance](http://www.ethercat.org/download/conformance)) explains the most important details on the topic and gives advice for preparation of the Conformance Test.

With passing the EtherCAT Conformance Test successfully a “Conformance Tested” certificate is issued and thus, the vendor may label his device with the official conformance test mark and use the term for advertisement for the certified device exclusively.

4.8 Vendor ID

Each EtherCAT compliant device has to implement the worldwide unique Vendor ID assigned by the EtherCAT Technology Group. The Vendor ID usage is covered by the Vendor ID Agreement (download from [www.ethercat.org](http://www.ethercat.org) → Member Area → Downloads → EtherCAT Technology Group Information).

The application for the ETG Vendor ID can be done online at [www.ethercat.org](http://www.ethercat.org) → Member Area → Vendor ID.

The Vendor ID is free of charge

The EtherCAT Vendor ID is mandatory to meet the Conformance Test requirements.
4.9 Step by Step Implementation

A typical approach of an EtherCAT implementation might look like the following:

- Become an ETG member (see clause 5)
- Purchase an evaluation or development board and an EtherCAT master (if not already included).
- There are also open source EtherCAT masters available (find more information at: [www.ethercat.org](http://www.ethercat.org) → Products → EtherCAT Master Devices)
- Attend EtherCAT Training Class (for dates see [www.ethercat.org](http://www.ethercat.org) → Events)
- Attend Evaluation Kit Workshop (for dates see [www.ethercat.org](http://www.ethercat.org) → Events)
- You may install software (e.g. EtherCAT master, monitoring tools) upfront to be prepared for the workshop. This helps you to use the time more efficiently.
- Set up a small EtherCAT system with master and evaluation board, maybe also some additional I/Os. The Master requires a standard PC with standard network card (100 MBit/s Full duplex).
- Built lab wiring between evaluation board and the application controller you want to use (e.g. 16 Bit µC).
- Start to build your software based on the Slave Sample Code
- Download Slave Sample Code in target hardware and set system into operation
- Start and test your hardware design
- Apply for an EtherCAT Vendor ID (see clause 4.8)
- Test software implementation for PDO and mailbox communication
- Software implementation of entire required functionality
- Use EtherCAT Conformance Test tool to test your device with every new EtherCAT feature implemented.
- System test, interoperability test (e.g. at EtherCAT Plug Fest), pilot applications/field test
- Certify your device at an EtherCAT Conformance Test Lab
4.10 Technical Support

Technical support throughout the development process is provided by the EtherCAT Technology Group predominately by the headquarters in Germany, but also by the various ETG offices worldwide (depending on local capacity). If you need direct contact, please address your specific question to the ETG (see contacts in clause 6.1).

Before contacting ETG for support, we expect reading the mentioned documentation above as well as the recently listed information below. We strongly recommend visiting one of the EtherCAT workshops and/or seminars for developers when starting an EtherCAT implementation.

Also a good opportunity to ask for technical experience with EtherCAT and for technical questions is provided by the EtherCAT Knowledge Base and the EtherCAT Forum within the member section of the EtherCAT website.

4.10.1 EtherCAT Knowledge Base

This is a constantly growing reference source for EtherCAT technology, containing the following subjects among others:

- FAQs
- EtherCAT Glossary
- Technology Description
- Guidelines
- Protocol Enhancements
- Application Notes
- Recommendations
- Profiles
- Examples

EtherCAT Knowledge Base online:
www.ethercat.org → Member Area → Knowledge Base

4.10.2 EtherCAT Forum

To discuss the EtherCAT technology, every ETG member is invited to discuss the EtherCAT technology and post own requests there. A lot of practical questions already answered in one of the following forum topics:

- EtherCAT Specification
  - Proposals
- Implementing EtherCAT
  - Master and Slave Devices
  - Evaluation Kit Hardware and Software
- EtherCAT Slave Conformance Test
  - Test Cases
  - Slave Conformance Test Tool
- EtherCAT Technology Group
  - ETG Services
  - New Downloads
- Ethercat.org Homepage
  - Suggestions for improvements and comments

EtherCAT Forum online:
www.ethercat.org → Member Area → Forum
4.10.3 Request for Support

Please read the following instructions to ensure that the inquiry is well prepared. This leads to a faster response time and helps us to improve the support.

Please explain the issue as detailed as necessary, but as simple as possible:

- What exactly is the problem?
- When does the problem occur?
- Can you reproduce the problem? How (Step by Step description)?
- Which software in which version is used? (master, operating systems, configuration tool, compiler, stacks… incl. versions)
- Which hardware is used? (master, slaves, network components, TAPs,…)
- What was tried to solve the problem, what happened then?
- Which information were found/read, are there questions on this information?

Please add additional information, if applicable:

- Wireshark scan for communication problems
  - Connect only the slave that causes the problem, no whole network scan
  - Capture the start up of the network (before the problem occurs)
  - Try to border the problem (e.g. problem occurs in frame #192,…)
  - At which point within your network did you capture the traffic? (on master, between master and first slave,…)
- *.tsm file if TwinCAT is used as master
- Sketch of hardware and testing equipment connected
- Screenshots of prompt errors and setting windows
- Anything else that helps to contain the issue
- Conformance Test Tool Project File in case of Conformance Testing
### 4.11 Useful Tools

Table 6 lists tools which might be helpful for an EtherCAT device development.

<table>
<thead>
<tr>
<th>Tool</th>
<th>Description and Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>EtherCAT Configurator</td>
<td>Configurator for reading and generating XML device description (EtherCAT Slave Information = ESI) and XML configuration descriptions (EtherCAT Network Information = ENI)</td>
</tr>
<tr>
<td></td>
<td>• Provided by Beckhoff Automation GmbH</td>
</tr>
<tr>
<td></td>
<td>• Alternatively: For development purposes an EtherCAT Hardware Configuration Tool (TwinCAT System Manager) is also delivered with the Beckhoff Evaluation Board</td>
</tr>
<tr>
<td></td>
<td>• → <a href="http://www.ethercat.org">www.ethercat.org</a> → Products → Development Systems, Tools and Services → Configuration Tools</td>
</tr>
<tr>
<td>EtherCAT Conformance Test Tool</td>
<td>The Conformance Test Tool allows to check protocol compliance in-house, e.g. as preparation for the official EtherCAT Conformance Test.</td>
</tr>
<tr>
<td></td>
<td>• The test tool is provided by Beckhoff Automation GmbH.</td>
</tr>
<tr>
<td></td>
<td>• Please contact Sandra Mimmler (<a href="mailto:s.mimmler@beckhoff.de">s.mimmler@beckhoff.de</a>)</td>
</tr>
<tr>
<td></td>
<td>• The test cases are defined and enhanced by the ETG and member companies in the working group “Conformance”</td>
</tr>
<tr>
<td>XML Editor</td>
<td>Used to edit/view EtherCAT Slave Information (ESI) file</td>
</tr>
<tr>
<td></td>
<td>• Any browser or text editor may be used</td>
</tr>
<tr>
<td></td>
<td>• More comfortable: Altova XML Spy (license fee required)</td>
</tr>
<tr>
<td></td>
<td>• Peter’s XML editor (freeware) → <a href="http://www.iol.ie/~pxe/">http://www.iol.ie/~pxe/</a></td>
</tr>
<tr>
<td></td>
<td>• XML Notepad (freeware)</td>
</tr>
<tr>
<td>Network Monitor</td>
<td>Wireshark (former Ethereal) can be used to monitor EtherCAT networks:</td>
</tr>
<tr>
<td></td>
<td>• Available for Linux and Windows</td>
</tr>
<tr>
<td></td>
<td>• EtherCAT Protocol analyser integrated since version &gt; 0.99.6a. Versions &lt; 0.99.6a need the EtherCAT protocol plug in (ethercat.dll) available at → <a href="http://www.ethercat.org">www.ethercat.org</a> → Downloads → EtherCAT Tools. Place it into the folder “..\Wireshark\plugins”</td>
</tr>
<tr>
<td></td>
<td>• Free download and further information: → <a href="http://www.wireshark.org">www.wireshark.org</a> → <a href="http://wiki.wireshark.org/Protocols/ethercat">wiki.wireshark.org/Protocols/ethercat</a></td>
</tr>
<tr>
<td>HexFile Editor</td>
<td>Any hex editor may be fine, here are two examples:</td>
</tr>
<tr>
<td></td>
<td>• HxD (freeware) → <a href="http://mh-nexus.de/en/hxd">http://mh-nexus.de/en/hxd</a></td>
</tr>
<tr>
<td></td>
<td>• TinyHexer (freeware) → <a href="http://www.mirkes.de">www.mirkes.de</a></td>
</tr>
<tr>
<td>HexFile Converter</td>
<td>Used to generate HexFile from pictures. The HexFile description of a picture may be used within the EtherCAT Slave Information (ESI) File.</td>
</tr>
</tbody>
</table>
5 EtherCAT Technology Group

The EtherCAT Technology Group is the forum in which key user companies from various industries and leading automation suppliers join forces to support, promote and advance the EtherCAT technology.

Goals

EtherCAT is an open technology. The EtherCAT Technology Group stands for this approach and ensures that every interested company may implement and use EtherCAT. At the same time the EtherCAT Technology Group aims to ensure the compatibility of EtherCAT implementations by defining functional requirements, conformance tests as well as certification procedures.

The Technology Groups goal is to ensure that EtherCAT technology meets and exceeds the requirements of the widest possible application range. In order to accomplish this goal the group combines leading control and application experts from machine builders, system integrators, end users and automation suppliers to provide both qualified feedback about application of the existing technology and proposals for future extensions of the specification.

The EtherCAT Technology Group organizes user and vendor meetings in which the latest EtherCAT developments are reviewed and discussed in regular periodical sessions.

Benefits

Group members get preferred access to specification drafts, specifications, white papers, prototype evaluation products and initial batch products and thus have a head start in evaluating, using or implementing the EtherCAT technology.

The members are eligible to participate in working groups and thus have influence on future enhancements of the EtherCAT technology specifications.

The member companies may use the EtherCAT and the EtherCAT Technology Group logos to show their support for this technology.

How to join the EtherCAT Technology Group

If you are interested in becoming a member of the EtherCAT Technology Group, please contact the ETG office for further information.

Membership Costs

The membership is free of charge, thus there are no annual membership fees. According the ETG by-laws a membership can only be introduced if the membership assembly decides so.
6 Appendix

6.1 EtherCAT Technology Group (ETG)

ETG Headquarters
Ostendstraße 196
90482 Nuremberg, Germany
Phone: +49 (911) 540 5620
Fax: +49 (911) 540 5629
Email: info@ethercat.org
Internet: www.ethercat.org

ETG Office North America
8108 Beauregard Drive
Volente, Texas 78641, USA
Phone: +1 877 ETHERCAT
Fax: +49 (512) 535 1437
Email: j.stubbs@ethercat.org

ETG Office Office China
Room 1608, Tower B
Investment Plaza, No. 27 Financial Street
Xicheng District
Beijing 100032, P.R. China
Phone: +86 (10) 66 21 7688
Fax: +86 (10) 66 21 0992
Email: b.fan@ethercat.org.cn

ETG Office Japan
Yusen Iwamotocho Bldg. 3F
2-3-3 Iwamoto-cho Chiyoda-ku
Tokyo 101-0032, Japan
Phone: +81 (3) 5825 5566
Fax: +81 (3) 5825 8550
Email: info.jp@ethercat.org

ETG Office Korea
Tri-TEK Corp.
717 DaeRyung TechnoTown III,
448 KasanDong Kumcheongu
Seoul 153-803, Korea
Phone: +82 (2) 2107 3240
Fax: +82 (2) 2107 3969
Email: keyyoo@ethercat.org

6.2 Help us to improve this document

You miss your own product in the products section? You found an error? You think some points have
to be explained more precisely?
Then please do not hesitate to contact us and thus help us to improve and complete this document.